16. The method of claim 9, wherein the gate stack comprises a gate dielectric, and wherein the gate dielectric is in contact with a top surface of the second silicon germanium layer.

17. The method of claim 9, wherein the second recesses comprise bottom surfaces at an intermediate level between a top surface and a bottom surface of the first silicon germanium layer.

18. The method of claim 4, wherein the recessing the isolation regions stops before a top surface of the recessed isolation regions is lowered to a level of an interface between the first silicon germanium layer and the second silicon germanium layer.

19. The method of claim 1, wherein the recessing the second silicon germanium layer stops before the first silicon germanium layer is exposed.

20. The method of claim 9, wherein the recessing the portions of the isolation regions stops before a top surface of the recessed isolation regions is lowered to a same level as an interface between the first silicon germanium layer and the second silicon germanium layer.

21. The method of claim 6, wherein the recessing the second silicon germanium layer stops after the first silicon germanium layer is exposed to the recesses.

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